What is laim d is:

1. A nonvolatile semiconductor memory device, comprising:

a group of memory cells formed in X and Y directions in and on a semiconductor substrate, the X and Y directions crossing each other, each memory cell including source and drain regions formed in the substrate, a first insulating film formed on a surface of the substrate between the source and drain regions, a floating gate formed on the first insulating film, and a control gate formed above the floating gate via a second insulating film;

a plurality of wordlines each connected to the control gates of the memory cells in the X direction;

a plurality of sub-bit lines, each sub-bit line connected to a predetermined number of source and drain regions of the memory cells in the Y direction;

a plurality of main-bit lines extending in the Y direction, each main-bit line being connected to the sub-bit line in the Y direction, and

a plurality of dielectric layers laminated on the sub-bit lines,

wherein each main-bit line is formed on any one of the plurality of dielectric layers, each main-bit line being connected to the corresponding sub-bit line via a conductive member penetrating through the dielectric layer under the

main-bit line, and adjacent two of the main-bit lines are located on different dielectric layers.

2. The nonvolatile semiconductor memory device of claim 1, wherein the sub-bit line is positioned between adjacent two of the memory cells in the X direction and comprises a first and second diffusion layers, the first diffusion layer being heavily impurity-doped and located below the floating gate of one memory cell to serve as the source region, the second diffusion layer being lightly impurity-doped and located below the floating gate of the other memory cell to serve as the drain region.

3. The nonvolatile semiconductor memory device of claim 1, wherein the main-bit line is made of a metal.

4. The nonvolatile semiconductor memory device of claim 1, wherein each main-bit line is formed directly above the sub-bit line connected thereto by the bit-line contact.

5. The nonvolatile semiconductor memory device of claim 1, wherein the dielectric layers consists of a first dielectric layer above the sub bit lines and a second dielectric layer on the first dielectric layer, wherein the main bit lines consist of a plurality of first-layer main-bit lines formed on the first

dielectric layer and a plurality of second-layer main-bit lines formed on the second dielectric layer, wherein the conductive member connecting the second-layer main-bit line and the corresponding sub-bit line consists of

a first member passing through the first dielectric layer, a second member passing through the second dielectric layer and a connection pad to connect the first member and the second member, the connection pad being formed on the first dielectric layer.

6. The nonvolatile semiconductor memory device of claim 5, wherein the second-layer main-bit line is arranged directly above the first-layer main-bit line provided with a laterally extended connection portion, wherein the first member is located perpendicularly on the sub-bit line, wherein the second member is located perpendicularly under the connection portion of the main-bit line.

7. The nonvolatile semiconductor memory device of claim 5, wherein the connection pad is made of the same material as that used for the first-layer main-bit line and is formed simultaneously with the formation thereof.

8. A process for producing a nonvolatile semiconductor memory device comprising the steps of:

(a) forming a group of memory cells in X and Y directions crossing each other in and on a semiconductor substrate, the formation of the memory cells including forming source and drain regions of each memory cell in the substrate, forming a plurality of sub-bit lines each in a stripe shape in the substrate, each sub-bit line connecting a predetermined number of source and drain regions in the Y direction, forming a first insulating film, a floating gate, a second insulating film and a control gate on a surface of the substrate between the source and drain regions, and forming a plurality of wordlines each in a stripe shape, each wordline connecting the control gates in the X direction;

(b) forming a first dielectric layer on the memory cells;

(c) forming a plurality of first conductive members in the first dielectric layer, each first conductive member being connected electrically to the sub-bit line and extending to an upper surface of the first dielectric layer;

(d) forming a plurality of first-layer main-bit lines and a plurality of connection pads on the first dielectric layer, each first-layer main-bit line being connected to the first conductive member and arranged in a stripe shape along the Y direction, each connection pad being connected to the first conductive member ;

(e) forming a second dielectric layer on the first dielectric layer, the first-layer main-bit lines and the

connection pads;

(f) forming a plurality of second conductive members in the second dielectric layer, each second conductive members being connected electrically to the connection pad and extending to an upper surface of the second dielectric layer; and

(g) forming a plurality of second-layer main-bit lines on the second dielectric layer, each second-layer main-bit line being connected to the second conductive member and arranged in a stripe shape along the Y direction.